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12EC029

First Semester M.Tech. Degree Examination, February 2013
Digital Circuits and Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Define the following:
   i) Threshold element
   ii) Threshold function
   iii) Unate function
   iv) Linearly separable function
   v) Linear separability. **(05 Marks)**

b. Show that a threshold logic realization of a full-adder requires only two threshold elements (Note: both sum and carryout must be generated). **(08 Marks)**

c. Given the switching function: $F(x_1\ x_2\ x_3\ x_4) = \sum (2, 3, 6, 7, 10, 12, 14, 15)$. Find a minimal threshold logic realization. **(07 Marks)**

2 a. Explain preset experiments with an example. **(08 Marks)**

b. Given the fault table of Table Q.2(b), design an adaptive decision tree. Explain the design procedure in detail. **(08 Marks)**

c. Write a note on path sensitizing. **(04 Marks)**

Table Q.2(b)

Tests	Faults							o/p of fault free circuit
	f_0	f_1	f_2	f_3	f_4	f_5	f_6	
T_1						1	1	0
T_2		1		1		1		1
T_3					1	1		0
T_4			1	1				1
T_5		1					1	0
T_6		1		1			1	1

3 a. Define Boolean difference of a function. **(02 Marks)**

b. Apply Boolean difference method to test the fault at x_3 for s – a – 0 and s – a – 1. **(08 Marks)**

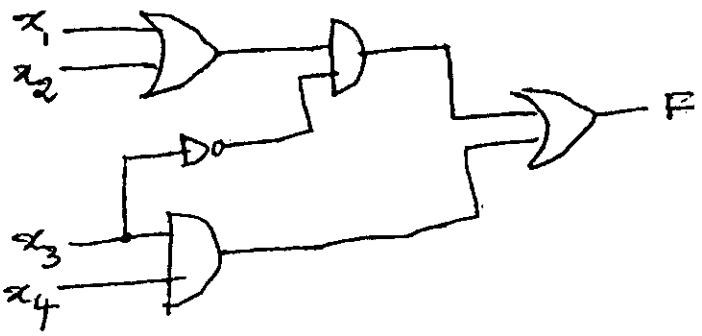

Fig.Q.3(b)

c. Given f(wxyz) = w'y' + y'z + wxz + xyz', generate a-tests and b-tests for multiple fault detection. **(10 Marks)**

4 a. Give the quadded realization of T = (AB + CD) (E + F). **(06 Marks)**

b. List the capacities and limitations of finite state machines. **(04 Marks)**

c. Define the following:

i) Synchronous sequential machine
ii) Distinguishable states.
iii) K-distinguishable
iv) Equivalent states
v) Compatible states
vi) Cover or contain. **(06 Marks)**

d. Give steps of Moore-Minimization procedure. **(04 Marks)**

5 a. Find the minimal form of machine M1 and give both reduced form of the state table and standard form of state table of machine M1. Refer Table Q.5(a). **(10 Marks)**

Machine M1

PS	NS, Z	
	x = 0	x = 1
A	E, 0	C, 0
B	C, 0	A, 0
C	B, 0	G, 0
D	G, 0	A, 0
E	F, 1	B, 0
F	E, 0	D, 0
G	D, 0	G, 0

Table Q.5(a)

Machine M2

PS	NS, Z	
	x = 0	x = 1
A	A, 0	C, 0
B	B, 0	B, -
C	B, 0	A, 1

Table Q.5(b)

b. Find augmented machine and corresponding minimal machines of Table Q.5(b). Machine M2. **(07 Marks)**

c. What do you mean by i) Maximal compatible; ii) Closed set; iii) Closed covering. **(03 Marks)**

6 a. Explain merger graph. Write the merger graph for the machine M3 shown in Table Q.6(a), thus find the set of maximal compatibles. **(10 Marks)**

Table Q.6(a)
Machine M3

PS	NS, Z			
	I_1	I_2	I_3	I_4
A	-	C, 1	E, 1	B, 1
B	E, 0	-	-	-
C	F, 0	F, 1	-	-
D	-	-	B, 1	-
E	-	F, 0	A, 0	D, 1
F	C, 0	-	B, 0	C, 1

b. Define the following:

i) Closed partitions
ii) Output-consistent partition
iii) Input-consistent partition
iv) Autonomous clock
v) Closed implication graph
vi) Partition pair. **(06 Marks)**

c. Write a note on Lattice of closed partions. **(04 Marks)**

7 a. Construct the π - lattice of machine M4 given in Table Q.7(a). **(10 Marks)**

Table Q.7(a)
Machine M4

PS	NS	
	x = 0	x = 1
A	E	B
B	E	A
C	D	A
D	C	F
E	F	C
F	E	C

b. Explain an application of states splitting to parallel decomposition with an example. **(10 Marks)**

8 a. Define homing sequence and write the homing tree for the machine M5 given in Table Q.8(a) **(10 Marks)**

Table Q.8(a)
Machine M5

PS	NS, Z	
	x = 0	x = 1
A	B, 0	D, 0
B	A, 0	B, 0
C	D, 1	A, 0
D	D, 1	C, 0

b. Describe the following:
   i) Distinguishing experiments.
   ii) Machine identification. **(10 Marks)**

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